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### **REMARKS**

Claims 1-21, 23-25 and 27-35 are pending in the application. Claims 1, 12 and 29 have been amended to include a feature of claim 21 and, therefore, do not present any new issues of patentability. Claims 36 and 37 have been added herein. Claim 36 presents original claim 10 in independent form and, therefore, does not present any new issues of patentability. Entry of the amendments and favorable reconsideration of the application, as amended, is respectfully requested.

#### ***I. REJECTION OF CLAIMS 1-21, 23-25 AND 27-35 UNDER 35 USC §103***

Claims 1-6, 8-21, 23-25 and 27-35 stand rejected under 35 USC §103(a) based on U.S. Patent No. 5,963,970 to *Davis* in view of U.S. Patent No. 5,963,909 to *Warren et al.* (hereinafter *Warren*). Claim 7 stands rejected under 35 USC §103(a) based on *Davis* and *Warren* in view of U.S. Patent No. 6,122,434 to *Sawabe*. Withdrawal of the rejection is respectfully requested for at least the following reasons.

Independent claim 1 has been amended to include a feature of original claim 21. Amended claim 1 recites an information update count managing method that includes a read step of reading out a last piece of information which has been written in the information storage area within a predetermined permitted update count. *The predetermined permitted update count is stored in non-volatile memory in a sector which includes a first program to be executed after a reset.* This is advantageous, for example, in that if one attempts to overwrite the predetermined usage count, the first program to be executed after a reset also is overwritten. By overwriting the first program to be executed after a reset, the microprocessor is not properly initialized, which can render the system inoperable.

In addressing claim 21, the Examiner, citing to column 4, lines 10-41 and Fig. 3 of *Davis*, contends that *Davis* teaches to provide the information storage area in a same sector as an initialization operation program, which is a first program to be executed after a reset. The Examiner additionally states that *Davis* clearly discloses a storage

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flash block reserved for erase count value and an update circuit, perhaps support software, modifying the wear-bar block for updating the erase count value at a proper time.<sup>1</sup>

Applicants respectfully disagree with the Examiner's continued assertion that *Davis* teaches an information storage area in a same sector as an initialization operation program, which is a first program to be executed after a reset. With reference to Fig. 3 of *Davis* (reproduced at right) and the cited portion of *Davis*, a flash memory device 140 is shown that includes a storage section 200 and a wear bar section 220. The wear bar section includes two wear bar blocks 230, 240, which keep track of the number of erasures for each flash storage block. *Davis* further discloses that the flash memory device 140 requires well known hardware, and perhaps support software, to control the setting of

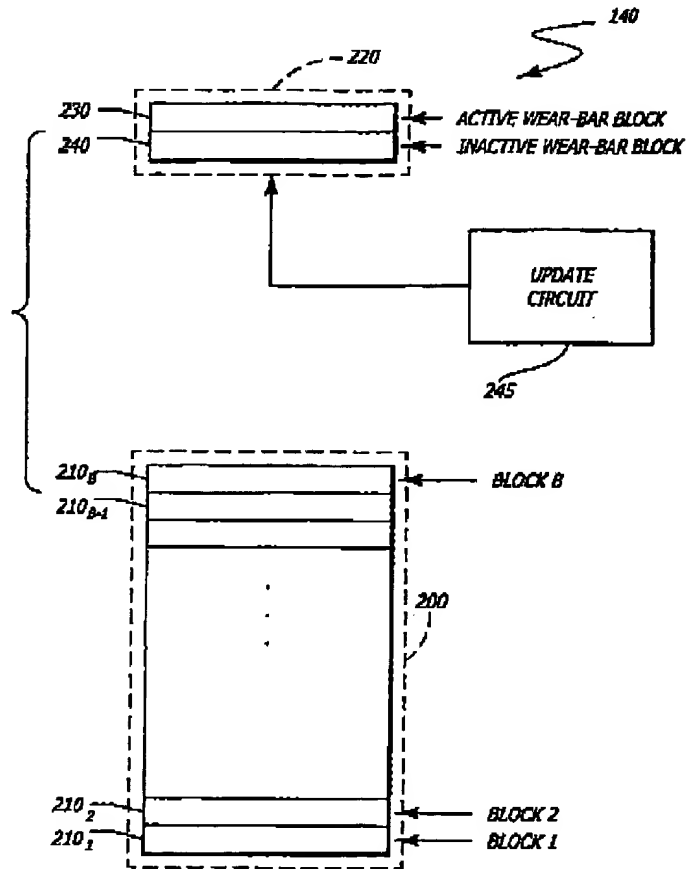


FIG. 3

<sup>1</sup> Page 11, first full paragraph of the Office Action

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bits representing the erase count values within wear-bar storage elements of wear-bar blocks as well as the manipulation of data between multiple wear-bar blocks.<sup>2 3</sup>

Thus, *Davis* discloses a wear-bar section 220 for keeping track of the number of times the flash memory is erased, and that the wear-bar section requires hardware, and perhaps support software, to control the setting of bits in the wear-bar section. *Davis* discusses the support software in conjunction with an update circuit. *Davis* clearly shows that an update circuit 245 is external from the wear-bar section 220. Thus, a reasonable conclusion is that the support software also is external from the wear-bar section 220. Nowhere in the cited portion, however, does *Davis* disclose that the support software is the first program executed after a reset. Additionally, nowhere in the cited portion does *Davis* disclose that the support software is stored in the same sector as the wear-bar blocks 220, 230.

The Examiner contends that *Davis* clearly shows the information storage area in a same sector 220 (figure 3), in which an update circuit, perhaps support software, modifying the wear-bar at a proper time. Applicant respectfully submits that Fig. 3 is a block diagram and, without more, one cannot reasonably infer that the support software is in the same sector as the wear-bar section 220. Contrary to the Examiner's opinion, a more reasonable interpretation of Fig. 3 is that the support software is part of the update circuit, which is external to the wear-bar section 220, as discussed above.

*Davis* has not been shown to teach or suggest that the *predetermined permitted update count is stored in the non-volatile memory in a sector which includes a first program to be executed after a reset*, as recited in claim 1 of the present application. *Warren* and *Sawabe* have not been shown to make up for the deficiencies of *Davis*.

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<sup>2</sup> Column 3, line 64 through column 4, line 3 of *Davis*

<sup>3</sup> Applicant notes that the update circuit 245 shown in Fig. 3 is believed to be the "well known hardware" referred in in the disclosure, although no reference to 245 is found in the disclosure

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Accordingly, withdrawal of the rejection of claim 1 is respectfully requested.

The above argument also applies to independent claims 12, 21, 25 and 29. Additionally, claims 21 and 25 recite a contents usage count stored in a contents usage count storage area. A contents usage count, as defined in the specification, is a count of the number of plays and copies made (see page 3, lines 20-21). In stark contrast, *Davis* is directed to the number of erase cycles.

Accordingly, withdrawal of the rejection of claims 12, 21, 25 and 29 is respectfully requested.

Claims 2-11, 13-20, 23, 24, 27, 28 and 30-35 directly or indirectly depend from one of the above independent claims and, therefore, can be distinguished from *Davis* and *Warren* for at least the same reasons.

Claim 30 depends from claim 29 and further recites that the boot area includes a check program for checking the contents of the information storage area. The Examiner contends that since *Davis* discloses support software to control the setting within the information area so that the boot area obviously comprises a check program for checking contents of the information storage area. Applicants respectfully disagree with the Examiner.

The present invention discloses a boot area that includes a check program for checking contents of the information storage area. The advantage of this feature is that if tampering has been performed in the information storage area, then it is possible to assure that the contents of the information storage area are trustworthy at the time when control is transferred to the system control program.<sup>4</sup>

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<sup>4</sup> See, e.g., page 29, line 24 through page 30, line 1 of the specification

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*Davis* simply discloses that the support software controls the setting of bits in the wear-bar section. Nowhere has it been shown that the support software disclosed in *Davis* is in a boot area, nor has it been shown that *Davis* teach or suggest *checking the information storage area*. *Davis* has not been shown to teach or suggest that the *boot area* further comprises a check program for *checking contents of the information storage area*, as recited in claim 30 of the present application.

Accordingly, withdrawal of the rejection of claims 2-11, 13-20, 23, 24, 27, 28 and 30-35 is respectfully requested.

## **II. Claims 36 and 37**

Claim 36 is original claim 10 written in independent form and, therefore, does not introduce new matter. Claim 36 recites an information update count managing method having a write step that includes a step of storing, in an update count storage area, the number of times information has been written in the information storage area.

In rejecting original claim 10, the Examiner admitted that *Davis* differs from the claimed invention in not specifically teaching for reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count. The Examiner contended, however, that *Warren* discloses this feature.

*Warren* describes a multi-media copy management system that includes two stages. A first stage is implemented at the master source level and consists of embedding a Standard Master Tag (SMT) into a data source, e.g., embedding an SMT into audio and/or video data prior to mass production of media containing the audio and/or video data. A second stage is implemented in a player/recorder copy management unit 150. The player/recorder 150 receives a Standard Copy Tag (SCT) data signal via a terminal 160, and searches the combined signal stored on the media

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to detect the presence of SMT data, which may have been inserted at the master source level, and/or SCT data, which previously may have been inserted by the player/recorder, e.g., inserted during a previous copy operation.<sup>5</sup> The player/recorder compares the data in the SMT and SCT to a Valid Copy Threshold (VCT), which indicates the number of allowed copies that may be made. If the data in the SMT and/or SCT is less than the VCT, then the player recorder permits copying of the data. During the record process, the copied data receives an updated SCT to reflect the next generation of the data. If the data in the SMT and/or SCT exceeds the VCT, then additional copies of the data are not permitted.<sup>6</sup>

Thus, *Warren* discloses a system in which the *number of additional copies* that may be made are stored in the media. *Warren*, however, does not disclose writing in an update count storage area of the non-volatile memory the *number of times pieces of information have been written in the information storage area*, as recited in original claim 10 and new claim 36.

Claim 37 depends from claim 36 and further recites that the step of storing includes initializing a plurality of bits in the update count storage area such that the plurality of bits are assigned to be "1", and releasing one of the plurality of bits to be "0" each time information is written in the information storage area. The cited art has not been shown to disclose the features of claim 37.

Accordingly, claims 36 and 37 are believed to be allowable.

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<sup>5</sup> See column 5, lines 35-57 of *Warren*

<sup>6</sup> See column 10, line 61 through column 11, line 4 of *Warren*

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### III. CONCLUSION

Accordingly, all claims are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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